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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/624,716
	Filing Date	July 21, 2003
	First Named Inventor	Luan C. Tran
	Art Unit	2812
	Examiner Name	Jennifer Kennedy
Total Number of Pages in This Submission	Attorney Docket Number	MI22-2357

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Firm or Individual	Jennifer J. Taylor, Ph.D.; Reg. No. 48,711; Wells St. John P.S.
Signature	<i>Jennifer J. Taylor</i>
Date	<i>November 11/2003</i>

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/624,716
Filing Date July 21, 2003
Inventor Luan C. Tran
Assignee Micron Technology, Inc.
Group Art Unit 2812
priority Examiner Kennedy, Jennifer J.
Attorney's Docket No. MI22-2357
Title: Methods of Forming Semiconductor Constructions

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References –See Attached Form PTO-1449

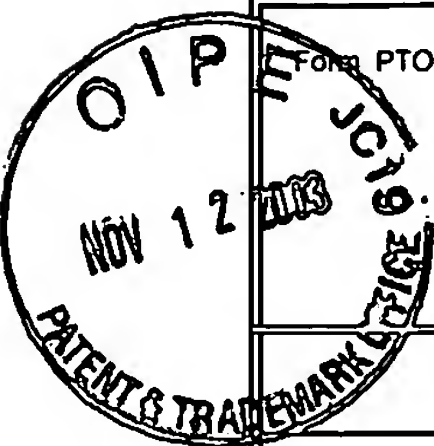
The attached form PTO-1449 is submitted in compliance with 37 CFR § 1.56. Copies of the cited art are included with the exception of U.S. patents and published U.S. applications (Official Gazette Notice: 05 August 2003). No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed within three months of the filing date of the application or before the mailing date of a first Office Action, whichever occurs last. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. § 1.17(p) to Deposit Account No. 23-0925.

Respectfully submitted,

Dated: November 11, 2003

By: Jennifer J. Taylor
Jennifer J. Taylor, Ph.D.
Reg. No. 48,711



Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2357		SERIAL NO. 10/624,716	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan C. Tran			
				FILING DATE July 21, 2003		GROUP 2812	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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							Yes No
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	AR		Watanabe, H. et al., <i>Novel 0.44μm² Ti-Salicide STI Cell Technology for High-Density NOR Flash Memories and High Performance Embedded Application</i> , IEEE 1998, pp. 36.2.1 - 36.2.4.				
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EXAMINER				DATE CONSIDERED			
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>							

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2812

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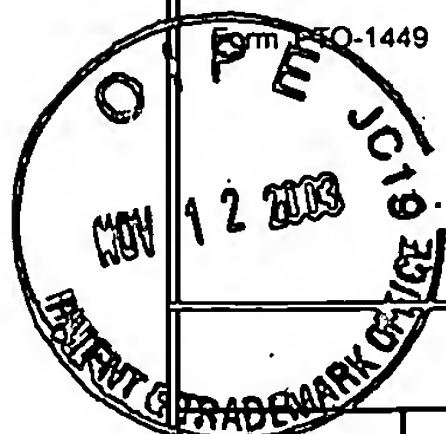
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	AT		Wolf, S., "Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Lattice Press 1986, pp. 434-437.

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	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AM							
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	AS							
	AT							

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